Maximum Mean Weight Cycle in a Graph and Gigahertz Processors

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The computer industry announces that they will put on the market around the year 2000 a gigahertz processor, that is a chip which runs with a cycle time of one nanosecond. This is not only a great challenge in technology, even a greater challenge for application of mathematics in VLSI design. The timing graph of a microprocessor is a directed graph with several billion edges, where the edges model the signal processing through combinatorial logic between 2 latches (nodes of the graph). The latches are governed by clock signals. If the total travel time of the signal on an edge is at most one nanosecond, deviations of even a few picoseconds due to design errors, technology, production, etc. matter substantially. The latches are controled by clock signals.

We have modelled the minimization problem of the cycle time of a microprocessor as an extended maximum mean weight cycle problem in a graph. By this, we cannot only minimize the cycle time or maximize the frequency of the microprocessor, but also take into consideration different process variations, clock jitters, balancing problems, early mode problems.

Of course, the classical maximum mean weighted cycle problems in graph had to be modified for this. However, by this approach we find the maximum frequency of a microprocessor under the given constraints. It turned out that without this application of combinatorial optimization industry would be unable to produce microprocessors with cycle times around one nanosecond.